AF 2186

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/609,567
Filing Date	June 30, 2000
First Named Inventor	Robert D. Bateman
Art Unit	2186
Examiner Name	T. Thai
Attorney Docket Number	042390.P9220

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  - -Brief in Support of Appeal (16 pages) (and two copies)
  - -Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Kenneth M. Seddon, Reg. No. 43,105 Intel Corporation
Signature	Kenneth M. Seddon
Date	September 22, 2003

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Lisa M. Hopkinson		
Signature	Lisa M. Hopkinson	Date	September 22, 2003

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 320.00

Complete if Known	
Application Number	09/609,567
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0221

Deposit Account Name: Intel Corporation

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =	X	=
Independent Claims		- 3** =	X	=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320.00
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 320.00

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	Kenneth M. Seddon	Registration No. *(Attorney/Agent)*	43,105	Telephone	480-554-9732
Signature	Kenneth M. Seddon			Date	September 22, 2003

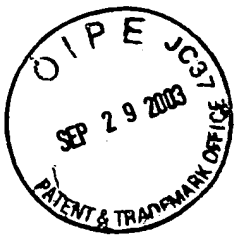
WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Patent Application

#13
10-8-03
AH



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	)	September 22, 2003
	)	
Robert D. Bateman	)	
	)	
Serial No.: 09/609,567	)	Group Art Unit: 2186
	)	
Filed: June 30, 2000	)	Examiner: T. Thai

RECEIVED
OCT 0 1 2003
Technology Center 2100

For: **CACHE HAVING A PRIORITIZE REPLACEMENT TECHNIQUE AND METHOD THEREFOR**

HONORABLE COMMISSIONER FOR PATENTS, PO Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF

IN SUPPORT OF APPELLANTS' APPEAL

TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Appellant (hereafter "Appellant") hereby submits this Brief in triplicate in support of their Appeal from a final decision by the Examiner in the above-captioned case. Appellant respectfully request consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, ON: 22 September 2003
Date of Deposit

INTEL CORPORATION
Name of Assignee

Lisa Marie Hopkinson 22 September 2003
SIGNATURE DATE

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-22 are currently pending in the above-referenced patent application. Claims 1-22 were rejected in the Final Office Action mailed on November 19, 2002 and are the subject of this appeal.

Claims 1-22 stand rejected under 35 U.S.C. §102(e) as being anticipated by Tischler et al. (US 2001/0049771 A1).

IV. STATUS OF AMENDMENTS

To the best of Appellant's knowledge, no amendments have been filed subsequent to the Final Rejection.

A copy of all claims on appeal, namely claims 1-22, is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

Simply stated, this application is related to caches used is processing system, and more specifically, to techniques for replacing or loading data into a cache for future use. When the processor requests an instruction or a piece of data, the request may be compared against a tag array to determine if the data requested is stored in the cache. If a match is found in the tag array, then the stored information or data may then be provided by the cache. If the requested information is not in the cache, then a cache "miss" has occurred and the information may have to be retrieved from other sources.

In some applications, it may be desirable to arrange the cache into sub-regions, commonly referred to as ways. This may provide more efficient use of the cache since portions of the cache may be designated to store more frequently requested information. If a cache miss has occurred, the information is retrieved from a slower memory source and stored in one of the ways of the cache. Appellant's invention provides techniques for locking at least some of the ways of the cache so that the locked way is not victimized (i.e. erased) when the new data is put into the cache. Traditional techniques simply replace or victimize the way in the cache that was least recently used (LRU). However, Appellant's invention provides more sophisticated and efficient techniques to updated caches.

Although the scope of Appellant's invention is not limited in this respect, Appellant's specification states with reference to Appellant's fig. 2 "In this particular embodiment, the highest priority is given to a way (e.g., one of ways 31-34) that is locked, although the scope of the present invention is not limited in this respect. For example, a way that is locked is given higher priority over the most recently accessed way. Thus, LRU update controller 90 may indicate that a locked way is the highest priority (e.g., most recently used) even though it has not been accessed by processor 110 during one of the recent requests for information." (page 11, line 21, to page 12, line 2). By prioritizing the lock way higher, the contents of that particular way may be protected from being replaced or victimized.

Claim 1

A method for storing data in a cache (e.g. cache 50) comprising:

prioritizing a locked way (e.g. way 21 of fig. 2) of the cache (e.g. cache 50) higher than a recently used way (e.g. way 22).

VI. ISSUES PRESENTED

A. Whether claims 1-22 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Tischler et al. (US 2001/0049771 A1) because Tischler fails to teach or suggest at least one feature of Appellant's invention.

B. Whether claims 1-22 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Tischler et al. (US 2001/0049771 A1) because Tischler fails to inherently teach at least one feature of Appellant's invention.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1-22 stand or fall together as Group I.

VIII. ARGUMENT

A. REJECTION OF CLAIMS 1-22 (GROUP I) UNDER 35 U.S.C. § 102(e) IN VIEW OF TISCHLER ET AL. IS IMPROPER. TISCHLER ET AL. DOES NOT EXPRESSLY MEET CLAIM LIMITATIONS DIRECTED TO "PRIORITIZING A LOCKED WAY HIGHER THAN A LEAST RECENTLY USED WAY."

The Final Office Action rejects claims 1-22 under 35 U.S.C. §102(e) as being anticipated by Tischler et al. (US 2001/0049771 A1

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Final Office Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Final Office Action has not succeeded in making a prima facie case.

Appellant begins with claim 1, which recites, among other things, **prioritizing** a locked way of the cache higher than a recently used way. Appellant respectfully submits that Tischler et al. cannot anticipate Appellant's claims because, at a minimum, Tischler et al. does not teach or suggest locking a way, and/or then prioritizing the locked way higher than a recently used way as explained for the reasons below.

Tischler et al. contains no express teaching or suggestion of prioritizing

To begin, the portion of Tischler et al. relied upon by the Examiner in the Final Office Action, namely page 5, contains no express teaching of prioritizing locked ways higher than other ways. The text of Tischler doesn't even mention the terms "prioritize", "prioritizing" or any derivative thereof.

Although the scope of Appellant's invention is not limited in this respect, Appellant's specification states "In this particular embodiment, the highest priority is given to a way (e.g., one of ways 31-34) that is locked, although the scope of the present invention is not limited in this respect. For example, a way that is locked is given higher priority over the most recently accessed way. Thus, LRU update controller 90 may indicate that a locked way is the highest priority (e.g., most recently used) even though it has not been accessed by

processor 110 during one of the recent requests for information." (page 11, line 21, to page 12, line 2). **As is clear from this example, prioritization relates to the ordering of the ways and is not specifically limited to just locking a way to prevent it from being victimized as suggested by the Examiner during the interview.**

Appellant respectfully points out that the relied upon portion of Tischler et al. does not contain any discussion of prioritizing, ranking, etc. of ways of a cache. Therefore, Tischler et al. cannot anticipate Appellant's claim 1 because Tischler et al. is devoid of the prerequisite teaching to establish a prima facie showing.

B REJECTION OF CLAIMS 1-22 (GROUP I) UNDER 35 U.S.C. § 102(e) IN VIEW OF TISCHLER ET AL. IS IMPROPER. TISCHLER ET AL. DOES NOT AND CANNOT INHERENTLY MEET CLAIM LIMITATIONS DIRECTED TO "PRIORITIZING A LOCKED WAY HIGHER THAN A LEAST RECENTLY USED WAY."

The Final Office action has not made the perquisite showing to rely on inherency

As demonstrated above, Tichler et al. does not contain any express teaching or suggestion of prioritizing a lock way higher than a way to be victimized in accordance with Appellant's claim 1. Furthermore, Final Office Action has conceded at least this point as the Final Office action is relying on inherency to demonstrate that this feature is taught or suggested by Tischler et al.

In particular, the Final Office Action stated on page 5, paragraph 5, that "... one **should** realize realize [sic] that the way being locked (way 1) **should** have higher priority that [sic] the non-locking ways." In other words, the Final Office Action suggests that one skilled in the art may interpret the reference to teach prioritizing in accordance with Appellant's claim 1 even though Tischler et al. does not expressly teach this feature.

However, the Court of Appeals for the Federal Circuit has stated repeatedly, that Inherency "may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *948 F.2d at 1269, 20 USPQ2d at 1749* (quoting I *n re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981)).*" Thus, in order to establish a prima facie showing, the Final Office Action must establish that Tischler et al. must teach prioritizing.

Appellant respectfully submits that, at a minimum, the rejection is improper because the Final Office Action has not demonstrated that the teaching or suggestion of prioritization must necessarily result. As explained above, and conceded by the Final Office Action, Tischler et al. does not contain any express teaching or suggestion of prioritizing or ranking. Since Tischler et al. does not teach this feature, Appellants respectfully submit that Tischler et al. cannot inherently disclose this feature. Thus, the Final Office Action's reliance upon inherency must be improper.

Appellant would also like to point out that a discussion of prioritizing ways is only found in Appellant's specification, not Tischler et al. However, as is well established, it is improper to rely on Appellant's specification as a basis for inherency.

Tischler et al. cannot inherently teach prioritization as this contrary to the express teaching of Tischler et al.

The CAFC has also establish that a feature cannot be inherent if the feature is not consistent with the express teachings of the relied upon document. For example, the Court of Appeals for the Federal Circuit recently reversed an Examiner's rejection that was based in part on inherency. See, In re Frank S. Glaug, 2002 U.S. App Lexis 4246 (Fed Cir. 2002).

In the present case, Appellant would like to point out that Tischler et al. teach in paragraph 62 that a locked way **is not prioritized higher than the other ways of the cache.** Tischler et al. teach that a "least recently used" LRU indicator is used to determine which of the ways in the cache is the least recently used. Tischler et al. further teach that the LRU algorithm may even identify that a locked way is the least recently used way – "Locking down a Way means that the Way is never replaced **regardless** of the "least recently used" use indicator" (emphasis added.)

Further, Tischler et al. teach that because the way is locked, it is not victimized even though the locked way was identified by the LRU algorithm as being the least recently used way. **In other words, Tischler et al. teaches that a locked way is not prioritized higher than the other ways when the LRU indicator is used, instead a locked way is considered by the LRU algorithm when determining what way in the cache is to be victimized.** The LRU algorithm cannot prioritize the locked way as part of the analysis. Thus, Tischler et al. teach away from Appellant's claimed invention.

Since Tischler et al. teach away from a feature of Appellant's claim 1, it cannot inherently teach prioritization as suggested by the Final Office Action. Appellant would also like to kindly point out that claims 13 and 20 recite prioritizing as well. Thus, these claims, along with the corresponding dependent claims, cannot be anticipated by Tischler et al. for at least the same reason.

Thus, Appellant respectfully submits that Tischler et al. cannot anticipate Appellant's claims 1-22 for at least these reasons.

IX. CONCLUSION

Appellants respectfully submit that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $320.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to Deposit Account No. 02-2666.

Respectfully submitted,

Date: 9-22-03 Kenneth M. Seddon

Kenneth M. Seddon
Attorney for Appellants
Registration Number: 43,105

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X. APPENDIX A: CLAIMS ON APPEAL

1. A method for storing data in a cache comprising:

prioritizing a locked way of the cache higher than a recently used way.

2. The method of claim 1, further comprising storing data in the recently used way.

3. The method of claim 1, further comprising:
prioritizing the locked way higher than a least recently used way; and
storing data in the least recently used way.

4. The method of claim 1, further comprising locking at least one way of the cache to provide the locked way.

5. The method of claim 1, further comprising reading data from a way of the cache prior to prioritizing the locked way, the way being the recently used way.

6. The method of claim 1, wherein prioritizing the locked way includes setting a bit in a register.

7. The method of claim 1, further comprising setting a bit in a register to indicate priority of the recently used way.

8. The method of claim 1, further comprising writing data to a way of the cache prior to prioritizing the locked way, the way being the recently used way.

9. The method of claim 1, further comprising:
locking a first way of the cache to provide the locked way; and
locking a second way of the cache to provide an additional locked way.

10. The method of claim 9, further comprising prioritizing the locked way higher than the additional locked way.

11. The method of claim 9, further comprising:

setting a first bit in a register to indicate priority of the locked way; and

setting a second bit in a register to indicate priority of the additional locked way.

12. The method of claim 11, further comprising setting a third bit in a register to indicate priority of the recently used way.

13. A method comprising:

locking a first way of a cache;

accessing a second way of the cache;

accessing a third way of the cache;

prioritizing the first way of the cache higher than the second way of the cache; and

writing data to the second way of the cache

14. The method of claim 13, wherein locking the first way includes setting a bit in a register to indicate the priority of the first way.

15. The method of claim 13, wherein writing data to the second way occurs if the second way has been accessed more recently than the first way.

16. The method of claim 15, wherein writing data to the second way occurs if the second way has been accessed more recently than the third way.

17. An apparatus comprising a cache having a first way and a second way, the apparatus comprising:

a circuit adapted to write data to the first way if the first way has been accessed more recently than the second way.

18. The apparatus of claim 17, wherein the circuit if further adapted to lock the second way.

19. The apparatus of claim 17, further comprising a memory location adapted to indicate the priority of the first way and the second way.

20. An article comprising:

a machine readable storage medium having stored thereon instructions capable of being executed by a data processing platform, said instructions being adapted to prioritize a locked way of a cache higher than a least recently used way of the cache.

21. The machine readable storage medium of claim 20, wherein said instructions are further adapted to set a bit in a memory location to indicate the priority of the locked way and the least recently used way.

22. The machine readable storage medium of claim 21, wherein said instructions are further adapted to store data in the least recently used way.